REMARKS

Summary of the Office Action

Claims 1-31 are pending in the above-identified patent application.

The Examiner has rejected claims 1, 2, 4, 7-10, 12-17, 22, 27, and 30 under 35 U.S.C. § 102(b) as being anticipated by Agrawal et al. U.S. Patent No. 5,740,069. Claims 18-21 and 23-26 have been rejected under 35 U.S.C. § 103(a) as being obvious from Agrawal in view of Schlecher et al. U.S. Patent No. 6,366,120.

Each of claims 3, 5, 6, and 11 has been objected to as being dependent upon a rejected base claim, but allowable subject matter has been indicated. Claims 28, 29, and 31 have been allowed.

Summary of Applicants' Reply

Applicants note with appreciation the allowance of claims 28, 29, and 31 and the indication of allowable subject matter in claims 3, 5, 6, and 11. Applicants expressly reserve the right to rewrite any one or more of claims 3, 5, 6, and 11 in independent form if its respective base claim is not ultimately allowed. The Examiner's rejections and objection are respectfully traversed.

Applicants' Reply to the Prior Art Rejections

Claims 1, 2, 4, 7-10, 12-17, 22, 27, and 30 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Agrawal. Claims 18-21 and 23-26 have been rejected under 35 U.S.C. § 103(a) as being obvious from Agrawal in view of Schlecher. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by independent claim 1, relates to a programmable logic device that includes a plurality of logic elements (LEs), at least one input/output (I/O) block, and a signal routing architecture for routing signals among the LEs and the at least one I/O

block. The signal routing architecture includes a plurality of horizontal and vertical signal routing conductors, at least one block input multiplexer for selectively providing signals from the routing conductors to the at least one I/O block, and at least one output bypass path for providing a direct connection between an output of an LE and the at least one I/O block. Independent claim 27 defines a programmable logic device with similar features, and independent claim 30 relates to a method whose features correspond to those of claim 1. The references cited by the Examiner, whether taken singly or in combination, neither show nor suggest the claimed invention.

Applicants' invention, as defined by independent claim 1, includes "at least one block input multiplexer for selectively providing signals from said plurality of horizontal and vertical signal routing conductors to said at least one I/O block." Each of independent claims 27 and 30 includes a feature that corresponds to this feature of claim 1. For instance, claim 27 defines "programmable routing circuitry for programmably selecting from any of a plurality of signals in the interconnection circuitry a signal for application to the I/O circuit." Claim 30 defines "using a signal routing architecture that comprises at least one block input multiplexer for routing signals among said LEs and at least one I/O block." Applicants' specification describes this feature in connection with the illustrative embodiment of FIG. 3A:

> In operation, LAB 110 drives its output onto signal conductor 321 using DIM 341 and corresponding driver 342. In turn, this output is provided to adjacent I/O block 160 by way of signal conductors 321 and 333 and an I/O block input multiplexer (BIM) 351. It will be understood that BIM 351 is similar to LIM 301 described above, in that BIM 351 selects a signal from inputs 352-354 to provide to the input of I/O multiplexer 361. Additionally, as shown in FIG. 3A, the output of BIM 351 can be applied to more than one or each I/O multiplexer 361 of I/O block 160. Page 14, line 29 to page 15, line 6.

Thus, the block input multiplexer (BIM) selects a signal from the routing conductors to provide to the at least one I/O block. This BIM is bypassed by the at least one output bypass path of applicants' invention, which provides a direct connection between an output from an LE to the at least one I/O block. For example, as further discussed in connection with the illustrative embodiment of FIG. 3A, "output bypass path 370 provides a faster connection between the output of LAB 110 and I/O multiplexer 361 than is otherwise possible because the delays associated with a signal traveling through DIM 341 and BIM 351, for example, are avoided." Page 16, lines 3-8.

In contrast, Agrawal describes a programmable integrated circuit with configurable logic blocks (CLBs), configurable input/output blocks (IOBs), and an interconnect network for routing signals between the CLBs and IOBs. The Examiner contends that multiplexer 4501 of FIG. 45 and multiplexer 4603* of FIG. 46 show "at least one block input multiplexer for selectively providing signals from [a] plurality of . . . signal routing conductors to . . . at least one I/O block," as defined by applicants' independent claim 1. Applicants respectfully disagree. Multiplexers 4501 and 4603 each reside in their respective IOB. As such, they cannot provide signals from routing conductors <u>to</u> at least one I/O block, as defined by applicants' claim 1. Moreover, because multiplexers 4501 and 4603 each reside in their respective IOB, they would not be bypassed by a direct connection from a peripheral CLB to the IOB. In contrast, applicants' output bypass path bypasses the BIM of applicants' invention, substantially avoiding the delay of the BIM when the bypass path is used.

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* In page 2 of the Detailed Action, the Examiner cited element 4600 of FIG. 46 in connection with this rejection. However, because element 4600 is an I/O pad, applicants assume that the Examiner meant to cite multiplexer 4603 instead.

Thus, Agrawal does not show or suggest at least one block input multiplexer for selectively providing signals from a plurality of signal routing conductors to at least one I/O block, as defined by applicants' claim 1. Nor does Agrawal show or suggest the corresponding feature in either of applicants' claims 27 or 30. Schlecher, which was applied by the Examiner for the alleged teaching of specific elements of certain dependent claims, does not make up the deficiencies of Agrawal in failing to show or suggest the claimed invention.

For these reasons, applicants respectfully submit that independent claims 1, 27, and 30 are patentable. Accordingly, dependent claims 2, 4, 7-10, 12-17, and 22 are also patentable. Applicants respectfully request that the rejections to claims 1, 2, 4, 7-10, 12-17, 22, 27, and 30 be withdrawn.

Applicants' Reply to the Objection of Claims 3, 5, 6, and 11

For the reasons set forth above, applicants respectfully submit that independent claim 1 is patentable. Accordingly, each of dependent claims 3, 5, 6, and 11 should also be patentable. Applicants respectfully request that the objection to claims 3, 5, 6, and 11 be withdrawn.

Conclusion

For the reasons set forth above, applicants respectfully submit that this application is in condition

for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,

Robert R. Jackson
Reg. No. 26,188
Attorney for Applicants
Fish & Neave IP Group
Ropes & Gray LLP
Customer No. 36981
1251 Avenue of the Americas
New York, New York 10020-1105
Tel.: (212) 596-9000